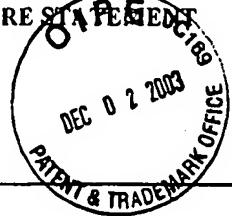


<b>FORM PTO - 1449</b> <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>				<b>ATTY DOCKET NO.:</b> ASC-023DVC2 <b>APPLICANTS:</b> Fitzgerald <b>SERIAL NO.:</b> 10/022,689 <b>FILING DATE:</b> December 17, 2001 <b>GROUP:</b> 2813				
<b>U.S. PATENT DOCUMENTS</b>								
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE	
	A1	4,010,045	03/01/1977	Ruehrwein				
	A2	4,710,788	12/01/1987	Dambkes et al.				
	A3	4,987,462	01/22/1991	Kim et al.				
	A4	4,990,979	02/05/1991	Otto				
	A5	5,013,681	05/07/1991	Godbey et al.				
	A6	5,155,571	10/13/1992	Wang et al.				
	A7	5,166,084	11/24/1992	Pfiester				
	A8	5,202,284	04/01/1993	Kamins et al.				
	A9	5,207,864	05/04/1993	Bhat et al.				
	A10	5,208,182	05/04/1993	Narayan et al.				
	A11	5,212,110	05/18/1993	Pfiester et al.				
	A12	5,221,413	06/22/1993	Brasen et al.				
	A13	5,241,197	08/31/1993	Murakami et al.				
	A14	5,285,086	02/08/1994	Fitzgerald, Jr.				
	A15	5,291,439	03/01/1994	Kauffmann, et al.				
	A16	5,310,451	05/10/1994	Tejwani et al.				
	A17	5,316,958	05/31/1994	Meyerson				
	A18	5,346,848	09/13/1994	Grupen-Shemansky et al.				
	A19	5,374,564	12/20/1994	Bruel				
	A20	5,413,679	05/09/1995	Godbey				
	A21	5,426,069	06/20/1995	Selvakumar et al.				
	A22	5,426,316	06/20/1995	Mohammad				
	A23	5,461,243	10/24/1995	Ek et al.				
	A24	5,461,250	10/24/1995	Burghartz et al.				
	A25	5,462,883	10/31/1995	Dennard et al.				
	A26	5,476,813	12/19/1995	Naruse				
	A27	5,479,033	12/26/1995	Baca et al.				
	A28	5,484,664	01/16/1996	Kitahara et al.				
	A29	5,523,243	06/04/1996	Mohammad				
	A30	5,523,592	06/04/1996	Nakagawa et al.				
<b>EXAMINER</b> <i>Inessa Schleifer</i>					<b>DATE CONSIDERED</b> <i>8/4/04</i>			

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		FILING DATE: December 17, 2001
		GROUP: 2813



## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
Xle	A31	5,536,361	07/16/1996	Kondo et al.			
Xle	A32	5,540,785	07/30/1996	Dennard et al.			
Xle	A33	5,596,527	01/12/1997	Tomioka, et al.			
Xle	A34	5,617,351	04/01/1997	Bertin, et al.			
Xle	A35	5,683,934	11/04/1997	Candelaria			
Xle	A36	5,698,869	12/16/1997	Yoshimi et al.			
Xle	A37	5,728,623	03/17/1998	Mori			
Xle	A38	5,739,567	04/14/1998	Wong			
Xle	A39	5,759,898	06/02/1998	Ek et al.			
Xle	A40	5,777,347	07/07/1998	Bartelink			
Xle	A41	5,786,612	07/28/1998	Otani et al.			
Xle	A42	5,786,614	07/28/1998	Chuang, et al.			
Xle	A43	5,792,679	08/11/1998	Nakato			
Xle	A44	5,808,344	09/15/1998	Ismail et al.			
Xle	A45	5,847,419	12/08/1998	Imai et al.			
Xle	A46	5,877,070	03/02/1999	Goesele et al.			
Xle	A47	5,906,708	05/25/1999	Robinson et al.			
Xle	A48	5,912,479	06/15/1999	Mori et al.			
Xle	A49	5,943,560	08/24/1999	Chang et al.			
Xle	A50	5,963,817	10/05/1999	Chu et al.			
Xle	A51	5,966,622	10/12/1999	Levine et al.			
Xle	A52	5,998,807	12/07/1999	Lustig et al.			
Xle	A53	6,013,134	01/11/2000	Chu et al.			
Xle	A54	6,033,974	03/07/2000	Henley et al.			
Xle	A55	6,033,995	03/07/2000	Muller			
Xle	A56	6,058,044	05/02/2000	Sugiura et al.			
Xle	A57	6,074,919	06/13/2000	Gardner et al.			
Xle	A58	6,096,590	08/01/2000	Chan et al.			
Xle	A59	6,103,559	08/15/2000	Gardner et al.			
Xle	A60	6,111,267	08/29/2000	Fischer et al.			

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EXAMINER <i>Waerea Schlett</i>	DATE CONSIDERED <i>8/4/04</i>
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<b>FORM PTO - 1449</b>		ATTY DOCKET NO.: ASC-023DVC2
<b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>		APPLICANTS: Fitzgerald
		SERIAL NO.: 10/022,689
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**U.S. PATENT DOCUMENTS**

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>Ale</i>	A61	6,117,750	09/12/2000	Bensahel et al.			
<i>Ale</i>	A62	6,130,453	10/10/2000	Mei, et al.			
<i>Ale</i>	A63	6,133,799	10/17/2000	Favors, Jr., et al.			
<i>Ale</i>	A64	6,140,687	10/31/2000	Shimomura et al.			
<i>Ale</i>	A65	6,143,636	11/07/2000	Forbes, et al.			
<i>Ale</i>	A66	6,153,495	11/28/2000	Kub et al.			
<i>Ale</i>	A67	6,154,475	11/28/2000	Soref et al.			
<i>Ale</i>	A68	6,160,303	12/12/2000	Fattaruso			
<i>Ale</i>	A69	6,162,688	12/19/2000	Gardner et al.			
<i>Ale</i>	A70	6,184,111	02/06/2001	Henley et al.			
<i>Ale</i>	A71	6,191,007	02/20/2001	Matsui et al.			
<i>Ale</i>	A72	6,191,432	02/20/2001	Sugiyama et al.			
<i>Ale</i>	A73	6,194,722	02/27/2001	Fiorini et al.			
<i>Ale</i>	A74	6,204,529	03/20/2001	Lung, et al.			
<i>Ale</i>	A75	6,207,977	03/01/2001	Augusto			
<i>Ale</i>	A76	6,210,988	04/03/2001	Howe et al.			
<i>Ale</i>	A77	6,218,677	04/17/2001	Brockaert			
<i>Ale</i>	A78	6,232,138	05/15/2001	Fitzgerald et al.			
<i>Ale</i>	A79	6,235,567	05/22/2001	Huang			
<i>Ale</i>	A80	6,242,324	06/05/2001	Kub et al.			
<i>Ale</i>	A81	6,249,022	06/19/2001	Lin, et al.			
<i>Ale</i>	A82	6,251,755	06/26/2001	Furukawa et al.			
<i>Ale</i>	A83	6,261,929	07/01/2001	Gehrke et al.			
<i>Ale</i>	A84	6,266,278	07/24/2001	Harari, et al.			
<i>Ale</i>	A85	6,271,551	08/07/2001	Schmitz et al.			
<i>Ale</i>	A86	6,271,726	08/07/2001	Fransis et al.			
<i>Ale</i>	A87	6,313,016	11/06/2001	Kibbel et al.			
<i>Ale</i>	A88	6,316,301	11/13/2001	Kant			
<i>Ale</i>	A89	6,323,108	11/27/2001	Kub et al.			
<i>Ale</i>	A90	6,329,063	12/11/2001	Lo et al.			

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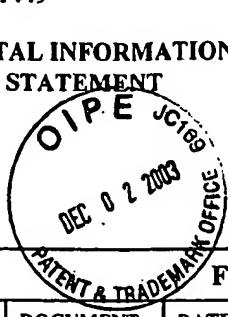
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<b>FORM PTO - 1449</b> <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>					ATTY DOCKET NO.: ASC-023DVC2			
					APPLICANTS: Fitzgerald SERIAL NO.: 10/022,689 FILING DATE: December 17, 2001 GROUP: 2813			
<b>U.S. PATENT DOCUMENTS</b>								
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE	
A91		6,335,546	01/01/2002	Tsuda et al.			07/30/1999	
A92		6,339,232	01/15/2002	Takagi			09/20/1999	
A93		6,368,733	04/09/2002	Nishinaga			08/05/1999	
A94		6,372,356	04/16/2002	Thornton et al.			04/028/2000	
A95		6,399,970	06/04/2002	Kubo et al.			09/16/1997	
A96		6,407,406	06/18/2002	Tezuka			06/29/1999	
A97		6,425,951	07/30/2002	Chu et al.			08/06/1999	
A98		6,429,061	08/06/2002	Rim			07/26/2000	
A99		6,420,937	07/16/2002	Akatsuka et al.			06/14/2001	
A100		6,521,041	02/18/2003	Wu et al.			04/09/1999	
A101		6,555,839	04/29/2003	Fitzgerald			05/16/2001	
A102		6,583,015	06/24/2003	Fitzgerald et al.			08/06/2001	
A103		6,521,041	02/18/2003	Wu et al.			04/09/1999	
A104		2001/0003364	06/14/2001	Sugawara et al.			12/08/2000	
A105		2002/0043660	04/18/2002	Yamazaki et al.			06/25/2001	
A106		6,593,191	07/15/2003	Fitzgerald			05/16/2001	
A107		6,573,126	06/03/2003	Cheng et al.			08/10/2001	
A108		2002/0096717	07/25/2002	Chu et al.			01/25/2001	
A109		2002/0100942	08/01/2001	Fitzgerald et al.			06/19/2001	
A110		2002/0123167	09/05/2002	Fitzgerald			07/16/2001	
A111		2002/0123183	09/05/2002	Fitzgerald			07/16/2001	
A112		2002/0123197	09/05/2002	Fitzgerald et al.			06/19/2001	
A113		2002/0125471	09/12/2002	Fitzgerald et al.			12/04/2001	
A114		2002/0125497	09/12/2002	Fitzgerald			07/16/2001	
A115		6,603,156	08/05/2003	Rim			03/31/2001	
A116		2003/0003679	01/02/2003	Doyle et al.			06/29/2001	

EXAMINER <i>hansen Selby</i>	DATE CONSIDERED <i>8/4/04</i>
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FORM PTO - 1449  SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT					ATTY DOCKET NO.: ASC-023DVC2  APPLICANTS: Fitzgerald SERIAL NO.: 10/022,689 FILING DATE: December 17, 2001 GROUP: 2813				
O I P E J C 189 P A T E N T & T R A D E M A R K O F F I C E DECEMBER 02 2003 FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<i>RL</i>	B1	41 01 167	07/23/1992	DE				NO	NO
<i>RL</i>	B2	0 587 520	03/16/1994	EP				NO	YES
<i>RL</i>	B3	0 683 522	11/22/1995	EP				NO	YES
<i>RL</i>	B4	0 828 296	03/11/1998	EP				NO	YES
<i>RL</i>	B5	0 829 908	03/18/1998	EP				NO	YES
<i>RL</i>	B6	0 838 858	04/29/1998	EP				NO	NO
<i>RL</i>	B7	1 020 900	07/19/2000	EP				NO	YES
<i>RL</i>	B8	1 174 928	01/23/2002	EP				NO	YES
<i>RL</i>	B9	2 342 777	04/19/2000	GB				YES	YES
<i>RL</i>	B10	10-270685	10/09/1998	JP				NO	YES
<i>RL</i>	B11	11-233744	08/27/1999	JP				NO	NO
<i>RL</i>	B12	2000-021783	08/31/2000	JP				NO	YES
<i>RL</i>	B13	2000-031491	01/28/2000	JP				NO	NO
<i>RL</i>	B14	2001-319935	11/16/2001	JP				NO	YES
<i>RL</i>	B15	2002-076334	03/15/2002	JP				NO	YES
<i>RL</i>	B16	2002-164520	06/07/2002	JP				NO	YES
<i>RL</i>	B17	2002-289533	10/04/2002	JP				NO	YES
<i>RL</i>	B18	4-307974	10/30/1992	JP				NO	NO
<i>RL</i>	B19	5-166724	07/02/1993	JP				NO	Abstract Only
<i>RL</i>	B20	6-177046	06/24/1994	JP				NO	Abstract Only
<i>RL</i>	B21	7-106446	04/21/1995	JP				NO	NO
<i>RL</i>	B22	7-240372	09/12/1995	JP				NO	Abstract Only
<i>RL</i>	B23	00/48239	08/17/2000	WO				NO	YES
<i>RL</i>	B24	00/54338	09/14/2000	WO				NO	YES

EXAMINER <i>Maura Schaff</i>	DATE CONSIDERED 8/4/04
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<b>FORM PTO - 1449</b> <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>					ATTY DOCKET NO.: ASC-023DVC2				
					APPLICANTS: Fitzgerald				
					SERIAL NO.: 10/022,689				
					FILING DATE: December 17, 2001				
					GROUP: 2813				
<b>FOREIGN PATENT DOCUMENTS</b>									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<i>Re</i>	B25	01/022482	03/29/2001	WO				NO	YES
<i>Re</i>	B26	01/54202	07/26/2001	WO				NO	YES
<i>Re</i>	B27	01/93338	12/06/2001	WO				NO	YES
<i>Re</i>	B28	01/99169	12/27/2001	WO				NO	YES
<i>Re</i>	B29	02/071488	09/12/2002	WO				NO	YES
<i>Re</i>	B30	02/071491	09/12/2002	WO				NO	YES
<i>Re</i>	B31	02/071495	09/12/2002	WO				NO	YES
<i>Re</i>	B32	02/082514	10/17/2002	WO				NO	YES
<i>Re</i>	B33	02/13262	02/14/2002	WO				NO	YES
<i>Re</i>	B34	02/15244	02/21/2002	WO				NO	YES
<i>Re</i>	B35	02/27783	04/04/2002	WO				NO	YES
<i>Re</i>	B36	02/47168	06/13/2002	WO				NO	YES
<i>Re</i>	B37	98/59365	12/30/1998	WO				NO	YES
<i>Re</i>	B38	99/53539	10/21/1999	WO				NO	YES
<i>Re</i>	B39	6-252046	11/19/1992	JP				NO	YES

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EXAMINER <i>hanna Seltz</i>	DATE CONSIDERED 8/4/04
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O P E R A T I O N S P A T E N T & T R A D E M A R K O F F I C E DECEMBER 2003 OTHER ART, JOURNAL ARTICLES, ETC.		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
<i>[Signature]</i>	C1	Armstrong et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEDM Technical Digest (1995 International Electron Devices Meeting) pp. 761-764.
<i>[Signature]</i>	C2	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices", PhD Thesis, Massachusetts Institute of Technology, 1999, pp. 1-154.
<i>[Signature]</i>	C3	Augusto et al., "Proposal for a New Process Flow for the Fabrication of Silicon-based Complementary MOD-MOSFETs without ion Implantation," Thin Solid Films, vol. 294, no. 1-2, pp. 254-258 (February 15, 1997).
<i>[Signature]</i>	C4	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," Modern Physics Letters B (2001) (abstract).
<i>[Signature]</i>	C5	Borenstein et al., "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," Proceedings of the 1999 12th IEEE International Conference on Micro Electro Mechanical Systems (MEMS) (January 17-21, 1999) pp. 205-210.
<i>[Signature]</i>	C6	Bouillon et al., "Search for the optimal channel architecture for 0.18/0.12 μm bulk CMOS Experimental study," IEEE, (1996) pp. 21.2.1-21.2.4.
<i>[Signature]</i>	C7	Bruel et al., "@SMART CUT: A Promising New SOI Material Technology," Proceedings 1995 IEEE International SOI Conference (October 1995) pp. 178-179.
<i>[Signature]</i>	C8	Bruel, "Silicon on Insulator Material Technology," Electronic Letters, Vol. 13, No. 14 (July 6, 1995) pp. 1201-1202.
<i>[Signature]</i>	C9	Bufler et al., "Hole transport in strained Si <sub>1-x</sub> Ge <sub>x</sub> alloys on Si <sub>1-y</sub> Ge <sub>y</sub> substrates," Journal of Applied Physics, Vol. 84, No. 10 (November 15, 1998) pp. 5597-5602.
<i>[Signature]</i>	C10	Burghartz et al., "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology", IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 1, January 1996, pp. 100-104.
<i>[Signature]</i>	C11	Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with strained epitaxial films," International Business Machines Corporation, USA (2002) (abstract).
<i>[Signature]</i>	C12	Carlin et al., "High Efficiency GaAs-on-Si Solar Cells with High Voc Using Graded GeSi Buffers," IEEE (2000) pp. 1006-1011
<i>[Signature]</i>	C13	Chang et al., "Selective Etching of SiGe/Si Heterostructures," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 202-204.
<i>[Signature]</i>	C14	Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," IEEE Electron Device Letters, Vol. 22, No. 7 (July 2001) pp. 321-323.
<i>[Signature]</i>	C15	Cheng et al., "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," Journal of Electronic Materials, Vol. 30, No. 12 (2001) pp. L37-L39.

EXAMINER <i>[Signature]</i>	DATE CONSIDERED <i>8/4/04</i>
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<b>FORM PTO - 1449</b>		<b>ATTY DOCKET NO.:</b> ASC-023DVC2
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		<b>SERIAL NO.:</b> 10/022,689
		<b>FILING DATE:</b> December 17, 2001
		<b>GROUP:</b> 2813
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>		
<b>EXAM. INIT.</b>	<b>OTHER DOCUMENTS:</b> (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C16	Cullis et al., "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," Journal of Vacuum Science and Technology A, Vol. 12, No. 4 (July/August 1994) pp. 1924-1931.
	C17	Currie et al., "Carrier mobilities and process stability of strained S in- and p-MOSFETs on SiGe virtual substrates," J. Vac. Sci. Technol. B., Vol. 19, No. 6 (Nov/Dec 2001) pp. 2268-2279.
	C18	Eaglesham et al., "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," Physical Review Letters, Vol. 64, No. 16 (April 16, 1990) pp. 1943-1946.
	C19	Feijoo et al., "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," Journal of Electronic Materials, Vol. 23, No. 6 (June 1994) pp. 493-496.
	C20	Fischetti et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," J. Appl. Phys., Vol. 80, No. 4 (August 15, 1996) pp. 2234-2252.
	C21	Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electronmobility in thin-oxide structures," Journal of Applied Physics, Vol. 89, No. 2 (January 15, 2001) pp. 1232-1250.
	C22	Fitzgerald et al., "Dislocation dynamics in relaxed graded composition semiconductors," Materials Science and Engineering B67, (1999) pp. 53-61.
	C23	Fitzgerald et al., "Relaxed GexSi <sub>1-x</sub> structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," AT&T Bell Laboratories, Murray Hill, NJ 07974 (1992) American Vacuum Society, pp. 1807-1819
	C24	Fitzgerald et al., "Totally Relaxed GexSi <sub>1-x</sub> Layers with Low Threading Dislocation Densities Grown on Si Substrates," Applied Physics Letters, Vol. 59, No. 7 (August 12, 1991) pp. 811-813.
	C25	Garone et al., "Silicon vapor phase epitaxial growth catalysis by the presence of germane," Applied Physics Letters, Vol. 56, No. 13 (March 26, 1990) pp. 1275-1277.
	C26	Gray and Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 1984, pp. 605-632.
	C27	Grützmacher et al., "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," Applied Physics Letters, Vol. 63, No. 18 (November 1, 1993) pp. 2531-2533.
	C28	Hackbarth et al., "Alternatives to thick MBE-grown relaxed SiGe buffers," Thin Solid Films, Vol. 369, No. 1-2 (July 2000) pp. 148-151.
	C29	Hackbarth et al., "Strain relieved SiGe buffers for Si-based heterostructure field-effect transistors," Journal of Crystal Growth, Vol. 201/202 (1999) pp. 734-738.
	C30	Herzog et al., "SiGe-based FETs: buffer issues and device results," Thin Solid Films, Vol. 380 (2000) pp. 36-41.
	C31	Höck et al., "Carrier mobilities in modulation doped Si <sub>1-x</sub> Gex heterostructures with respect to FET applications," Thin Solid Films, Vol. 336 (1998) pp. 141-144.

<b>EXAMINER</b>	<i>hanna Schulte</i>	<b>DATE CONSIDERED</b>	<i>8/4/04</i>
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FORM PTO - 1449  SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		ATTY DOCKET NO.: ASC-023DVC2  APPLICANTS: Fitzgerald  SERIAL NO.: 10/022,689  FILING DATE: December 17, 2001  GROUP: 2813
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
<i>JL</i>	C32	Höck et al., "High hole mobility in Si0.17 Ge0.83 channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," Applied Physics Letters, Volume 76, No. 26 (June 26, 2000) pp. 3920-3922.
<i>JL</i>	C33	Höck et al., "High performance 0.25 μm p-type Ge/SiGe MODFETs," Electronics Letters, Vol. 34, No. 19 (September 17, 1998) pp. 1888-1889.
<i>JL</i>	C34	Huang et al., "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," Applied Physics Letters, Vol. 76, No. 19 (May 8, 2000) pp. 2680-2682.
<i>JL</i>	C35	Huang et al., "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits", IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, July, 1998, pp. 1023-1036.
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<i>JL</i>	C37	IBM Technical Disclosure Bulletin, Volume 32, No. 8A, January 1990, "Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates", pp. 330-331.
<i>JL</i>	C38	Ishikawa et al., "Creation of Si-Ge-based SIMOX structures by low energy oxygen implantation," Proceedings 1997 IEEE International SOI Conference (October 1997) pp. 16-17.
<i>JL</i>	C39	Ishikawa et al., "SiGe-on-insulator substrate using SiGe alloy grown Si(001)," Applied Physics Letters, Vol. 75, No. 7 (August 16, 1999) pp. 983-985.
<i>JL</i>	C40	Ismail et al., "Modulation-doped n-type Si/SiGe with inverted interface," Appl. Phys. Lett., Vol. 65, No. 10 (September 5, 1994) pp. 1248-1250.
<i>JL</i>	C41	Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington, D.C. (December 10, 1995) pp. 20.1.1-20.1.4.
<i>JL</i>	C42	Kearney et al., "The effect of alloy scattering on the mobility of holes in a Si1-xGex quantum well," Semicond. Sci Technol., Vol. 13 (1998) pp. 174-180.
<i>JL</i>	C43	Kim et al., "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier", IEEE Microwave and Guided Wave Letters, Vol. 8, No. 8, August 1998, pp. 293-295.
<i>JL</i>	C44	Koester et al., "Extremely High Transconductance Ge/Si0.4Ge0.6 p-MODFET's Grown by UHV-CVD," IEEE Electron Device Letters, Vol. 21, No. 3 (March 2000) pp. 110-112.
<i>JL</i>	C45	König et al., "Design Rules for n-Type SiGe Hetero FETs," Solid State Electronics, Vol. 41, No. 10 (1997), pp. 1541-1547.
<i>JL</i>	C46	König et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters, Vol. 14, No. 4 (April 1993) pp. 205-207.
<i>JL</i>	C47	König et al., "SiGe HBTs and HFETs," Solid-State Electronics, Vol. 38, No. 9 (1995) pp. 1595-1602.
<i>JL</i>	C48	Kuznetsov et al., "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," J. Vac. Sci. Technol., B 13(6), pp. 2892-2896 (November/December 1995).
<i>JL</i>	C49	Larson, "Integrated Circuit Technology Options for RFIC's Present Status and Future Directions", IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, March 1998, pp. 387-399.

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<i>[Signature]</i>	C50	Lee and Wong, "CMOS RF Integrated Circuits at 5 GHz and Beyond", Proceedings of the IEEE, Vol. 88, No. 10, October 2000, pp. 1560-1571.
<i>[Signature]</i>	C51	Lee et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Si <sub>1-x</sub> Gex/Si virtual substrates," Applied Physics Letters, Vol. 79, No. 20 (November 12, 2001) pp. 3344-3346.
<i>[Signature]</i>	C52	Lee et al., "Strained Ge channel p-type MOSFETs fabricated on Si <sub>1-x</sub> Gex/Si virtual substrates," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A1.9.1-A1.9.5.
<i>[Signature]</i>	C53	Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A3.10.1-A3.10.6.
<i>[Signature]</i>	C54	Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," Journal of Applied Physics, Vol. 90, No. 6 (September 15, 2001) pp. 2730-2736.
<i>[Signature]</i>	C55	Leitz et al., "Hole mobility enhancements in strained Si/Si <sub>1-y</sub> Gey p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si <sub>1-x</sub> Gex (x<y) virtual substrates," Applied Physics Letters, Vol. 79, No. 25 (December 17, 2001) pp. 4246-4248.
<i>[Signature]</i>	C56	Li et al., "Design of high speed Si/SiGe heterojunction complementary metal-oxide-semiconductor field effect transistors with reduced short-channel effects," J. Vac. Sci. Technol., A Vol. 20 No.3 (May/June 2002) pp. 1030-1033.
<i>[Signature]</i>	C57	Lu et al., "High Performance 0.1 $\mu$ m Gate-Length P-Type SiGe MODFET's and MOS-MODFET's", IEEE Transactions on Electron Devices, Vol. 47, No. 8, August 2000, pp. 1645-1652.
<i>[Signature]</i>	C58	M. Kummer et al., "Low energy plasma enhanced chemical vapor deposition," Materials Science and Engineering B89 (2002) pp. 288-295.
<i>[Signature]</i>	C59	Maiti et al., "Strained-Si heterostructure field effect transistors," Semicond. Sci. Technol., Vol. 13 (1998) pp. 1225-1246.
<i>[Signature]</i>	C60	Mazzara, "Silicon-On-Insulator by Wafer Bonding: A Review," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 341-347.
<i>[Signature]</i>	C61	Meyerson et al., "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," Applied Physics Letters, Vol. 53, No. 25 (December 19, 1988) pp. 2555-2557.
<i>[Signature]</i>	C62	Mizuno et al., "Advanced SOI-MOSFETs with Strained-SI Channel for High Speed CMOS-Electron/Hole Mobility Enhancement," 2002 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, (June 13-15), IEEE New York, NY, pp. 210-211.
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<i>[Signature]</i>	C64	Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE IDEM Technical Digest, (1999 International Electron Device Meeting) pp. 934-936.

EXAMINER

*Karen Sletten*

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<i>JL</i>	C65	Nayak et al., "High-Mobility Strained-Si PMOSFET's"; IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1709-1716.
<i>JL</i>	C66	O'Neill et al., "SiGe Virtual substrate N-channel heterojunction MOSFETS," Semicond. Sci. Technol., Vol. 14 (1999) pp. 784-789.
<i>JL</i>	C67	Papananos, "Radio-Frequency Microelectronic Circuits for Telecommunication Applications", Kluwer Academic Publishers, 1999, pp. 115-117, 188-193.
<i>JL</i>	C68	O'ta, Y. et al., "Application of heterojunction FET to power amplifier for cellular telephone," ELECTRONIC LETTERS, IEE STEVANAGE, GB, Vol. 30 No. 11, 26 May 1994, pp. 906-907.
<i>JL</i>	C69	Parker et al., "SiGe heterostructure CMOS circuits and applications," Solid State Electronics, Vol. 43 (1999) pp. 1497-1506.
<i>JL</i>	C70	Ransom et al., "Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's," IEEE Transactions on Electron Devices, Vol. 38, No. 12 (December 1991) pp. 2695.
<i>JL</i>	C71	Reinking et al., "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," Electronics Letters, Vol. 35, No. 6 (March 18, 1999) pp. 503-504.
<i>JL</i>	C72	Rim et al., "Enhanced Hole Mobilities in Surface-channel Strained-Si p-MOSFETs"; IEDM, 1995, pp. 517-520.
<i>JL</i>	C73	Rim et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's"; IEEE Transactions on Electron Devices, Vol. 47, No. 7, July 2000, pp. 1406-1415.
<i>JL</i>	C74	Rim, "Application of Silicon-Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field-Effect Transistors", PhD Thesis, Stanford University, 1999; pp. 1-184.
<i>JL</i>	C75	Robbins et al., "A model for heterogeneous growth of Si <sub>1-x</sub> Ge <sub>x</sub> films for hydrides," Journal of Applied Physics, Vol. 69, No. 6 (March 15, 1991) pp. 3729-3732.
<i>JL</i>	C76	Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEEE Trans. Electron Devices (August 1996) pp. 1224-1232.
<i>JL</i>	C77	Schäffler, "High-Mobility Si and Ge Structures," Semiconductor Science and Technology, Vol. 12 (1997) pp. 1515-1549.
<i>JL</i>	C78	Sugimoto and Ueno, "A 2V, 500 MHz and 3V, 920 MHz Low-Power Current-Mode 0.6 $\mu$ m CMOS VCO Circuit", IEICE Trans. Electron., Vol.E82-C, No. 7, July 1999, pp. 1327-1329.
<i>JL</i>	C79	Ternent et al., "Metal Gate Strained Silicon MOSFETs for Microwave Integrated Circuits", IEEE October 2000, pp. 38-43.
<i>JL</i>	C80	Tweet et al., "Factors determining the composition of strained GeSi layers grown with disilane and germane," Applied Physics Letters, Vol. 65, No. 20 (November 14, 1994) pp. 2579-2581.
<i>JL</i>	C81	Usami et al., "Spectroscopic study of Si-based quantum wells with neighboring confinement structure," Semicon. Sci. Technol. (1997) (abstract).
<i>JL</i>	C82	Welser et al., "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," IEEE Electron Device Letters, Vol. 15, No. 3 (March 1994) pp. 100-102.

EXAMINER

*hannah schultz*

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<i>Xle</i>	C83	Welser, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors," PhD Thesis, Stanford University, 1994, pp. 1-205.
<i>Xle</i>	C84	Welser et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEEE IDEM Technical Digest (1992 International Electron Devices Meeting) pp. 1000-1002.
<i>Xle</i>	C85	Welser et al., "Evidence of Real-Space Hot-Electron Transfer in High Mobility, Strained-Si Multilayer MOSFETs," IEEE IDEM Technical Digest (1993 International Electron Devices Meeting) pp. 545-548.
<i>Xle</i>	C86	Wolf and Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, Lattice Press, Sunset Beach, CA, pp. 384-386 (1986).
<i>Xle</i>	C87	Xie et al., "Semiconductor Surface Roughness: Dependence on Sign and Magnitude of Bulk Strain," The Physical Review Letters, Vol. 73, No. 22 (November 28, 1994) pp. 3006-3009.
<i>Xle</i>	C88	Xie et al., "Very high mobility two-dimensional hole gas in Si/ Ge <sub>x</sub> Si <sub>1-x</sub> /Ge structures grown by molecular beam epitaxy," Appl. Phys. Lett., Vol. 63, No. 16 (October 18, 1993) pp. 2263-2264.
<i>Xle</i>	C89	Xie, "SiGe Field effect transistors," Materials Science and Engineering, Vol. 25 (1999) pp. 89-121.
<i>Xle</i>	C90	Yeo et al., "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel," IEEE Electron Device Letters, Vol. 21, No. 4 (April 2000) pp. 161-163.
<i>Xle</i>	C91	Zhang et al., "Demonstration of a GaAs-Based Compliant Substrate Using Wafer Bonding and Substrate Removal Techniques," Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, University Park, PA 16802 (1998) pp. 25-28.
<i>Xle</i>	C92	Tsang et al., "Measurements of alloy composition and strain in thin Ge <sub>x</sub> Si <sub>1-x</sub> layers," J. Appl. Phys., Vol. 75 No. 12 (June 15, 1994) pp. 8098-8108.
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<i>Xle</i>	C94	Yamagata et al., "Bonding, Splitting and Thinning by Porous Si in ELTRAN®, SOI-Epi Wafer™," Mat. Res. Soc. Symp. Proc., Vol. 681E (2001) pp. I8.2.1-I8.2.10.

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